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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,933	04/03/2001	Ming-Ren Lin	F0556	1551

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EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/824,933	Applicant(s) LIN, MING-REN
	Examiner Khiem D Nguyen	Art Unit 2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 11, 8.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

The non-final rejection as set forth in paper No. (7) is withdrawn in response to applicants' amendments.

A new rejection is made as set forth in this Office Action.

Claims (1-15 and 21-25) are pending in the application.

Drawings

The corrected or substitute drawings were received on 10-22-2002. These drawings are accepted by the examiner.

New Grounds of Rejection

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori et al. (U.S. Patent 6,252,294) in view of Mori et al. (U.S. Patent 5,162,241).

Hattori teaches a method of manufacturing a semiconductor device on a silicon-on-insulator wafer including a silicon active layer having at least two die pads 1a formed thereon, the at least two die pads separated by at least one scribe lane 1b, comprising the steps of (See col. 4, line 8 to col. 6, line 47 and FIGS. 1-5D):

forming at least one cavity 6 through the silicon active layer 4 in the at least one scribe lane (See FIG. 2) comprising forming a sidewall liner in the cavity (See col. 8, lines 53-57);

forming at least one gettering plug in each cavity 6, each gettering plug comprising doped fill material 7 containing a plurality of gettering sites wherein the doped fill material is polysilicon formed by LPCVD deposition of the polysilicon and a dopant in the cavity (See col. 5, lines 66-67);

Hattori discloses in FIG. 2 wherein the gettering plug 7 extends down through the silicon active layer 4, and contacts a dielectric insulation layer 3 on the wafer.

Hattori discloses in FIG. 3B-C wherein the gettering plug 7 extends down through both a silicon active layer 4 and a dielectric insulation layer 3 on the wafer.

Hattori fails to teach subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites wherein the gettering step gettered impurities migrate into a silicon substrate layer below the dielectric insulation layer as recited in present claims 1 and 8.

Mori discloses in (col. 2, lines 32-37 and FIG. 1A-G) subjecting the semiconductor wafer to conditions to getter at least one impurity into the gettering site wherein the gettering step gettered impurities migrate into a silicon substrate layer (FIG.1B, 1) below the dielectric insulation layer (FIG. 1B, 2). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Mori's teaching into Hattori's method in order to remove a contaminated layer of the gettering site in which the contaminant impurities are trapped (See col. 2, lines 32-37).

Neither Hattori nor Mori teaches wherein the dopant is phosphorous as recited in present claims 3-4. However, the use of phosphorous as a dopant is well-known to one of ordinary skill in the art of making semiconductor devices.

3. Claims 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori et al. (U.S. Patent 6,252,294) in view of Mori et al. (U.S. Patent 5,162,241).

Hattori teaches a method of gettering impurities on a silicon-on-insulator wafer including a silicon active layer having at least two die pads 1a formed thereon, the at least two die pads separated by at least one scribe lane 1b, comprising the steps of (See col. 4, line 8 to col. 6, line 47 and FIGS. 1-5D):

forming at least one cavity 6 through the silicon active layer 4 in the at least one scribe lane (See FIG. 2) comprising forming a sidewall liner in the cavity (See col. 8, lines 53-57);

filling the cavity with a fill material 7 comprises polysilicon (See col. 5, lines 66-67) and adding at least one dopant by one of codeposition and implantation to the fill material to form at least one gettering plug including a plurality of gettering sites;

Hattori discloses in FIG. 2 wherein the gettering plug 7 extends down through the silicon active layer 4, and contacts a dielectric insulation layer 3 on the wafer.

Hattori discloses in FIG. 3B-C wherein the gettering plug 7 extends down through both a silicon active layer 4 and a dielectric insulation layer 3 on the wafer.

Hattori fails to teach subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites wherein the gettering step gettered impurities

migrate into a silicon substrate layer below the dielectric insulation layer as recited in present claims 9 and 15.

Mori discloses in (col. 2, lines 32-37 and FIG. 1A-G) subjecting the semiconductor wafer to conditions to getter at least one impurity into the gettering site wherein the gettering step gettered impurities migrate into a silicon substrate layer (FIG.1B, 1) below the dielectric insulation layer (FIG. 1B, 2). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Mori's teaching into Hattori's method in order to remove a contaminated layer of the gettering site in which the contaminant impurities are trapped (See col. 2, lines 32-37).

Neither Hattori nor Mori teaches wherein the dopant is one or more selected from phosphorous, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon, and germanium as recited in present claims 10. However, the use of phosphorous, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon, and germanium as a dopant is well-known to one of ordinary skill in the art of making semiconductor devices.

4. Claims 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori et al. (U.S. Patent 6,252,294) in view of Mori et al. (U.S. Patent 5,162,241).

Hattori teaches a method of gettering impurities on a silicon-on-insulator wafer including a silicon active layer, buried oxide layer and a silicon substrate, the silicon active layer having at least two die pads 1a formed thereon, the at least two die pads separated by at least one scribe lane 1b wherein the wafer comprises a plurality of adjacent die pads and a single scribe lane separates each die pad from the adjacent die

pads and wherein the scribe lane comprises a pair of parallel rows of gettering plugs, comprising the steps of (See col. 4, line 8 to col. 6, line 47 and FIGS. 1-5D):

forming a plurality of cavities 6 through the silicon active layer 4 and the buried oxide layer 3 to the silicon substrate in the at least one scribe lane (See FIG. 2) comprising forming a sidewall liner in the cavity (See col. 8, lines 53-57);

filling the cavities with a fill material 7 comprises polysilicon (See col. 5, lines 66-67) and implanting at least one dopant into the fill material in the cavities to form at least one gettering plug including a plurality of gettering sites;

Hattori fails to teach subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites wherein in the gettering step, gettered impurities move into the silicon substrate as recited in present claims 21-22.

Mori discloses in (col. 2, lines 32-37 and FIG. 1A-G) subjecting the semiconductor wafer to conditions to getter at least one impurity into the gettering site wherein in the gettering step, gettered impurities move into the silicon substrate (FIG.1B, 1). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Mori's teaching into Hattori's method in order to remove a contaminated layer of the gettering site in which the contaminant impurities are trapped (See col. 2, lines 32-37).

Neither Hattori nor Mori teaches wherein the dopant is one or more selected from phosphorous, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon, and germanium as recited in present claims 25. However, the use of phosphorous, arsenic, antimony, bismuth, boron, aluminum, gallium, indium,

helium, neon, argon, krypton, xenon, and germanium as a dopant is well-known to one of ordinary skill in the art of making semiconductor devices.

Response to Amendment

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaudhuri Olik can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800

K.N.
December 17, 2002